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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,056	02/13/2004	Toshitomo Umei	2004_0180A	5630

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EXAMINER

CHU, WUTCHUNG

ART UNIT	PAPER NUMBER
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2619

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/777,056

Applicant(s)

UMEI ET AL.

Examiner

Wutchung Chu

Art Unit

2619

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 12/14/2005; 2/13/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
2. Claims 1-7, 10-16, and 19-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Shin et al., hereinafter Shin, (US2002/0159552).

Regarding claim 1, Shin discloses a method and system for plesiosynchronous communications with null insertion and removal (**see paragraph 73**) comprising:

- a processing unit (**see figure 3 box 3802 and box 3812 and paragraph 167 ASIC chip**) for processing transmission/reception data based on the communication protocol (**see paragraph 85 protocol**);
- a transmitting/receiving unit (**see paragraph 10 transmit and receive device**) for generating a transmission signal based on the transmission data processed by the processing unit and outputting the resultant signal (**see paragraphs 77 and 78 and figure 2 and paragraph 168**), and generating reception data based on a transmission signal output from other data transmission apparatus and outputting the resultant data to the processing unit (**see paragraph 84 the phase**

lock loop provides a timing signal to the transmitter for serial transmission of the symbols and provides multiple timing signals with different phases to the receiver for receiving the serially transmitted symbols and paragraph 81);

- **transmitting/receiving unit (see paragraph 10 transmit and receive device)**
initialization means for initializing the transmitting/receiving unit so that the transmitting/receiving unit is operable to perform transmission/reception with other transmitting/receiving units of other data transmission apparatuses (**see paragraphs 97 and 168-169**); and
- **processing unit (see figure 3 box 3802 and box 3812 and paragraph 167 ASIC chip)** initialization means for initializing (**see paragraph 97**) the processing unit so that the processing unit is operable to perform data communication with other processing units of other data transmission apparatuses via the transmitting/receiving unit (**see figure 2**) after the transmitting/receiving unit initialization means initializes the transmitting/receiving unit (**see paragraphs 102, 106, and 108**).

Regarding claims 2, 11, Shin the transmitting/receiving unit initialization means initializes the transmitting/receiving unit by establishing clock synchronization between the transmitting/receiving unit and other transmitting/receiving units of other data transmission apparatuses (**see paragraphs 97 and 169**).

Regarding claims 3, 12, Shin teaches:

- the transmitting/receiving unit (**see paragraph 10 transmit and receive device**) initialization means includes clock synchronization establishment notification means for notifying the processing unit initialization means of establishment of clock synchronization when the clock synchronization is established (**see paragraph 97**), and
- the processing unit (**see figure 3 box 3802 and box 3812 and paragraph 167 ASIC chip**) initialization means starts initialization, in response to clock synchronization establishment notification made by the clock synchronization establishment notification means, by which the processing unit is operable to perform data communication with other processing units (**see paragraph 84 the phase lock loop provides a timing signal to the transmitter for serial transmission of the symbols and provides multiple timing signals with different phases to the receiver for receiving the serially transmitted symbols and paragraph 81**) of other data transmission apparatuses via the transmitting/receiving unit (**see paragraph 108**).

Regarding claims 4, Shin teaches

- if no clock synchronization establishment notification is made by the clock synchronization establishment notification means within a predetermined time, the processing unit initialization means starts initialization so that the

processing unit is operable to perform data communication with other processing units of other data transmission apparatuses via the transmitting/receiving unit **(see paragraph 98)**,

- the processing unit initialization means further includes communication anomaly detection means for detecting anomalies of data communication during the started initialization **(see paragraph 73 overrun condition or underrun condition)**, and
- when the communication anomaly detection means detects the anomalies **(see paragraph 73 overrun condition or underrun condition)**, the transmitting/receiving unit initialization means re-performs initialization by which clock synchronization is established between the transmitting/receiving unit and other transmitting/receiving units of other data transmission apparatuses **(see paragraphs 73 and 97)**.

Regarding claims 5 and 14, Shin teaches

- the transmitting/receiving unit generates the transmission signal by mapping the transmission data to any of a plurality of signal levels **(see paragraph 78)**, and
- the transmitting/receiving unit initialization means performs initialization **(see paragraphs 97 and 108)** by causing the transmitting/receiving unit:

- to transmit an initialization signal for identifying the signal levels to other data transmission apparatuses (**see paragraphs 82 and 97**); and
- to receive an initialization signal transmitted from other data transmission apparatus, and set evaluation levels for identifying a signal level of the transmission signal using the initialization signal (**see paragraphs 97 and 102**).

Regarding claims 6, 15, Shin teaches

- the transmitting/receiving unit initialization means includes evaluation level setting completion notification means for notifying the processing unit initialization means of completion of setting of evaluation levels when the evaluation levels are set (**see paragraph 97 and 102**), and
- the processing unit initialization means starts initialization, in response to notification of a completion of evaluation level setting made by the evaluation level setting completion notification means, by which the processing unit is operable to perform data communication with other processing units of other data transmission apparatuses via the transmitting/receiving unit (**see paragraphs 106-108**).

Regarding claims 7, 16, Shin teaches

- if no notification of a completion of evaluation level setting is made by the evaluation level setting completion notification means within a

predetermined time, the processing unit initialization means starts initialization so that the processing unit is operable to perform data communication with other processing units of other data transmission apparatuses via the transmitting/receiving unit (**see paragraph 108**),

- the processing unit initialization means further includes communication anomaly detection means for detecting anomalies of data communication during the started initialization (**see paragraph 73**), and
- when the communication anomaly detection means detects the anomalies, the transmitting/receiving unit initialization means re-performs initialization for setting the evaluation levels (**see paragraphs 73 and 97**).

Regarding claim 10, Shin discloses a method and system for plesiosynchronous communications with null insertion and removal (**see paragraph 73**) comprising:

- each data transmission apparatus (**see figure 38 box 3801 and 3811**) includes:
- a processing unit (**see figure 3 box 3802 and box 3812 and paragraph 167 ASIC chip**) for processing transmission/reception data based on a predetermined communication protocol (**see paragraph 85 protocol**);
- a transmitting/receiving unit (**see paragraph 10 transmit and receive device**) for generating a transmission signal based on the transmission data processed by the processing unit and outputting the resultant signal to other data transmission apparatus connected to a next stage (**see paragraphs 77 and 78**).

and figure 2 and paragraph 168), and generating reception data based on a transmission signal output from other data transmission apparatus connected to a previous stage and outputting the resultant data to the processing unit (see paragraph 84 the phase lock loop provides a timing signal to the transmitter for serial transmission of the symbols and provides multiple timing signals with different phases to the receiver for receiving the serially transmitted symbols and paragraph 81);

- transmitting/receiving unit (see paragraph 10 transmit and receive device) initialization means for initializing the transmitting/receiving unit so that the transmitting/receiving unit is operable to perform transmission/reception with other transmitting/receiving units of other data transmission apparatuses (see paragraphs 97 and 168-169; and
- processing unit (see figure 3 box 3802 and box 3812 and paragraph 167 ASIC chip) initialization means for initializing the processing unit so that the processing unit is operable to perform data communication with other processing units of other data transmission apparatuses via the transmitting/receiving unit (see figure 2) after the transmitting/receiving unit initialization means initializes the transmitting/receiving unit (see paragraphs 102, 106, and 108).

Regarding claim 13, Shin teaches:

- if no clock synchronization establishment notification is made by the clock synchronization establishment notification means within a predetermined time, the processing unit initialization means starts initialization so that the processing unit is operable to perform data communication with other processing units of other data transmission apparatuses via the transmitting/receiving unit (**see paragraph 98**),
- the processing unit initialization means further includes communication anomaly detection means for detecting anomalies of data communication during the started initialization (**see paragraph 73 overrun condition or underrun condition**), and
- when the communication anomaly detection means detects the anomalies (**see paragraph 73 overrun condition or underrun condition**), the transmitting/receiving unit initialization means re-performs initialization by which clock synchronization is established between the transmitting/receiving unit and other transmitting/receiving units of other data transmission apparatuses (**see paragraphs 73 and 97**).

Regarding claim 19, Shin teaches initialization method for initializing a data transmission apparatus (**see paragraph 10 transmit and receive device**) generating a transmission signal corresponding to data to be processed based on a predetermined communication protocol (**see paragraph 85 protocol**), and transmitting/receiving the

transmission signal to/from other data transmission apparatus (**see paragraph 10 transmit and receive device**), wherein

- a physical layer (**see paragraph 10 transmit and receive device**), which generates a transmission signal corresponding to transmission data processed based on the communication protocol and transmits the resultant signal (**see paragraphs 77 and 78 and figure 2 and paragraph 168**), and generates reception data based on a transmission signal output from other data transmission apparatus, and other physical layers of other data transmission apparatuses are initialized so as to be operable to transmit/receive the transmission signal (**see paragraphs 77 and 78 and figure 2 and paragraph 168**), and
- after initialization of the physical layers (**see paragraphs 77 and 78 and figure 2 and paragraph 168**), a link layer (**see figure 3 box 3802 and box 3812 and paragraph 167 ASIC chip**), which processes the transmission data and the reception data based on the communication protocol (**see paragraph 85 protocol**), and other link layers of other data transmission apparatuses (**see figure 38A box 3801 box 3811**) are initialized (**see paragraphs 97 and 168-169**) so as to be operable to perform data communication via the physical layers (**see paragraph 77**).

Regarding claim 20, Shin teaches initialization of the physical layer (**see paragraph 10 transmit and receive device**) is performed by establishing clock

synchronization between the physical layer and other physical layers of other data transmission apparatuses (**see paragraph 84 the phase lock loop provides a timing signal to the transmitter for serial transmission of the symbols and provides multiple timing signals with different phases to the receiver for receiving the serially transmitted symbols and paragraphs 81 and 97).**

Regarding claim 21, Shin teaches wherein

- the clock synchronization is established in initialization of the physical layer, establishment of the clock synchronization is notified (**see paragraphs and 82, 84, and 97), and**
- in response to notification of establishment of the clock synchronization, initialization is started so that the link layer and other link layers of other data transmission apparatuses are operable to perform data communication via the physical layer (**see paragraphs 84 and 108).**

Regarding claim 22, Shin teaches

- if no notification of establishment of the clock synchronization is made within a predetermined time, initialization is started so that the link layer and other link layers of other data transmission apparatuses are operable to perform data communication via the physical layer (**see paragraph 98), and**

- when anomalies (**see paragraph 73 overrun condition or underrun condition**) of data communication are detected during the started initialization, initialization for establishing clock synchronization between the physical layer and other physical layers of other data transmission apparatuses is re-performed (**see paragraphs 73 and 97**).

Regarding claim 23, Shin teaches

- the transmission signal is generated from the transmission data which is mapped to any of a plurality of signal levels by the physical layer (**see paragraph 78**), and
- initialization of the physical layer (**see paragraphs 97 and 108**) is performed by:
 - transmitting an initialization signal for identifying the signal levels, from the physical layer to other data transmission apparatuses(**see paragraphs 82 and 97**); and
 - setting evaluation levels for identifying a signal level of the transmission signal using an initialization signal after the physical layer receives the initialization signal transmitted from other data transmission apparatus (**see paragraphs 97 and 102**).

Regarding claim 24, Shin teaches

- in the initialization of the physical layer, notification of a completion of evaluation level setting is made when the evaluation levels are set (**see paragraph 97 and 102**), and
- in response to notification of a completion of evaluation level setting, initialization by which the link layer and other link layers of other data transmission apparatuses are operable to perform data communication via the physical layer is started (**see paragraphs 106-108**).

Regarding claim 25, Shin teaches

- if no notification of a completion of evaluation level setting is made within a predetermined time, initialization is started so that the link layer and other link layers of other data transmission apparatuses are operable to perform data communication via the physical layer (**see paragraph 108**), and
- when anomalies of data communication are detected during the started initialization, initialization for setting the evaluation levels is re-performed (**see paragraphs 73 and 97**).

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 8, 17, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Stolyarov et al., hereinafter Stolyarov, (US2004/0076435).

Regarding claims 8, 17 and 26, Shin disclose all the subject matter of the claimed invention with the exception of the communication protocol used by the processing unit is defined by MOST (Media Oriented Systems Transport).

Stolyarov from the same or similar fields of endeavor teaches the use of MOST (see **Stolyarov paragraph 54**). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the MOST as taught by Stolyarov in the system for plesiosynchronous communications with null insertion and removal of Shin in order to provide an improved device and procedure for transmitting and distributing audio signals in a vehicle (see **Stolyarov paragraphs 5 and 6**).

6. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Stillman et al., hereinafter Stillman, (US5551066).

Regarding claims 9 and 18, Shin teaches

- the processing unit and the transmitting/receiving unit separately include a phase lock loop (**see paragraph 84**) for performing a process by establishing clock synchronization (**see paragraph 97**), and
- each phase lock loop (**see paragraph 84**) included in the processing unit and the transmitting/receiving unit uses the reference frequency output

Shin discloses all the subject matter of the claimed invention with the exception of:

- further comprising a radiator for outputting a reference frequency, wherein

Stillman from the same or similar fields of endeavor teaches the use of radiator (**see Stillman figure 1**). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the radiator as taught by Stillman in the system for plesiosynchronous communications with null insertion and removal of Shin in order to provide improvement in communication amount nodes through walls, floors and other obstacles (**see Stillman col. 2 lines 28-44**).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ziv et al. (US4513370); Andre et al. (US2003/0161391); pedyash et al. (US2004/0217881); Mantey et al. (US2004/0230878); Si et al. (US7010612); Gulati et al. (US2004/0037313).

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wutchung Chu whose telephone number is 571 270 1411. The examiner can normally be reached on Monday - Friday 1000 - 1500EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan D. Orgad can be reached on 571 272 7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WC/
Wutchung Chu

EDAN D. ORGAD
SUPERVISORY PATENT EXAMINER

